Rule 126
~~20.~~ 31 (New) The assembly structure recited in claim ~~19~~ 30 wherein the first plurality of conductor lines are fabricated with first narrowing cross-section areas at points where the memory cells are capable of a permanent change of state.

Rule 126
~~21.~~ 32 (New) The assembly structure recited in claim ~~20,~~ 31 wherein the second plurality of conductor lines includes second narrowing cross-section areas configured to align with the first narrowing cross-section areas.

REMARKS

This application is under final rejection. Applicant has presented arguments herein below that Applicant believes should render the claims allowable. In the event, however, that the Examiner is not persuaded by Applicant's arguments, Applicant respectfully requests that the Examiner enter the amendment to clarify issues upon appeal.

This communication is in response to the Final Office Action dated December 17, 2002. Claims 1-18 are pending in the present Application. Claims 16 and 17 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 3 has been canceled. Claims 4 and 5 have been amended for clarification. Claims 19- 21 have been added and include the allowed subject matter. Claims 1, 2 and 4-21 remain pending in the present Application.

The present invention includes an assembly structure for a memory device comprising a substrate having at least one fold line thereon dividing the substrate into at

least two sections and a layer of memory arrays fabricated on each of the at least two sections, each section being disposed so that the memory arrays on sections adjacent to each other form an interface in which the memory arrays are aligned to provide at least one operable electronic device with the at least two sections folded on each other along the at least one fold line.

112 Rejections

Claims 3 and 4

The Examiner states:

> **Claims 3 and 4 are rejected under 35 USC 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**
>
> **Lines 1-2 in each of claims 3 and 4 recite the limitation "the sections of memory arrays". There is insufficient antecedent basis for this limitation in the claims.**

Applicant asserts that claim 3 has been canceled and claim 4 has been amended to overcome the above-referenced informalities. Consequently, the Examiner's 112 rejection is no longer applicable.

102 Rejections

1-5, 8, 10 and 11

For ease of review, Applicant reproduces independent claim 1 herein below:

1. An assembly structure for a memory device comprising:
a substrate having at least one fold line thereon, dividing the substrate into at least two sections; and
a layer of memory arrays fabricated on each of the at least two sections, each section being disposed so that the memory arrays on sections adjacent to each other form an interface in which the memory arrays are aligned to provide at least one operable

electronic device with the at least two sections folded on each other along the at least one fold line.

The Examiner states:

> **Nicewarner shows (see, e.g., figs 4 and 5) all aspects of the instant invention including an assembly structure for a memory device, said assembly structure comprising:**
>
> **a substrate 12 having at least one fold line 71 thereon, dividing the substrate into at least two sections**
>
> **a layer 32 of memory arrays fabricated on each of the two sections (see, e.g., fig. 3)**
>
> **Nicewarner further disposes each section so that the memory arrays on sections adjacent to each other form an interface in which the memory arrays are aligned to provide at least one operable electronic device with the at least two sections folded on each other along the fold line (see, e.g., fig 3).**

Applicant respectfully disagrees with the Examiner's rejection. The present invention of claim 1 recites an assembly structure for a memory device comprising a substrate having at least one fold line thereon dividing the substrate into at least two sections and a layer of memory arrays fabricated on each of the at least two sections, each section being disposed so that the memory arrays on sections adjacent to each other form ***an interface in which the memory arrays are aligned to provide at least one operable electronic device with the at least two sections folded on each other along the at least one fold line***. (Emphasis added.)

The Examiner asserts that Nicewarner shows all aspects of the instant invention including an assembly structure for a memory device. Applicant respectfully disagrees. Nicewarner discloses a three dimensional flexible assembly of integrated circuits and method of fabricating the assembly of circuits including a folded flexible substrate with integrated circuit chips. The invention has provisions for allowing mechanical and electrically functional attachment of integrated circuit chips to one or both sides of the

flexible substrate using flip chip assembly techniques. In addition, a rigid package substrate is provided upon which the folded substrate is secured with the associated chips. The chips are electrically connected to the flexible substrate and the flexible substrate is in turn electrically connected to the rigid substrate. A cover is also provided that covers and protects the flexible substrate and the associated chips as well as a portion of the connected rigid package substrate. In an additional embodiment, the cover and rigid substrate are omitted and instead the combined folded flexible substrate and integrated circuit chips are encapsulated with a suitable compound.

As recited in claim 1 of the present invention, the memory arrays are disposed on adjacent sections of the at least one fold line, such that ***an interface*** is formed in which the memory arrays are aligned to provide ***at least one operable electronic device*** with the at least two sections folded on each other ***along the at least one fold line***. (Emphasis added.) Applicant respectfully asserts that this combination of features is neither taught or suggested by the Nicewarner reference.

Referring to Figure 3 of Nicewarner (see Attached Exhibit A), the Examiner asserts that Nicewarner discloses a substrate **12** having at least one fold line **71** thereon, dividing the substrate into at least two section and a layer **32** of memory arrays fabricated on each of the two sections. The Examiner further asserts that Nicewarner disposes each section so that the memory arrays on sections adjacent to each other form an interface in which the memory arrays are aligned to provide at least one operable electronic device with the at least two sections folded on each other along the fold line. Applicant respectfully disagrees with the Examiner's characterization of the Nicewarner reference.

The Examiner equates portion **71** of Figure 3 to the at least one fold line of the recited invention. Applicant asserts that although portion **71** of Nicewarner divides the substrate **12** into at least two sections as recited in claim 1 of the present invention, Applicant fails to see ***an interface*** in which memory arrays are aligned to provide at least one operable electronic device with the at least two sections folded on each other ***along the at least one fold line.*** Stated another way, Nicewarner does not disclose an interface in which memory arrays are aligned to provide at least one operable electronic device with at least two sections folded on each other along portion **71.**

Applicant therefore asserts that since Nicewarner does not disclose an interface in which memory arrays are aligned to provide at least one operable electronic device with at least two sections folded on each other along the at least one fold line as recited in claim 1 of the present invention, claim 1 of the present invention is not anticipated by the Nicewarner reference. Consequently, claim 1 is allowable over the Examiner's cited reference.

Since claims 2-5, 8, 10 and 11 are dependent on claim 1, the above-articulated argument with regard to claim 1 applies with equal force to claims 2-5, 8, 10 and 11. Accordingly, claims 2-5, 8, 10 and 11 should be allowed over this reference.

Claims 12-15

For ease of review, Applicant reproduces independent claim 12 herein below:

12. An assembly structure for a memory device, comprising:
a common substrate having multiple sections;
a first layer of a memory array disposed on a first section of the multiple sections;
a second layer of a memory array disposed on a second section of the multiple sections;

at least one fold line disposed on the common substrate to define alignment of the memory arrays on the first and second sections; and

wherein the sections may be folded on each other at the fold line to form an operable electronic device in the memory device.

The Examiner states:

> **Nicewarner shows (see, e.g., figs 4 and 5) all aspects of the instant invention including an assembly structure for a memory device, said assembly structure comprising:**
>
> **a common substrate 12 having multiple sections**
>
> **a first layer 32 of a memory array disposed on a first section of the multiple sections**
>
> **a second layer 32 of a memory array disposed on a second section of the multiple sections**
>
> **at least one fold line 71 disposed on the common substrate 12 to define the alignment of the memory arrays on the first and second sections wherein the sections may be folded on each other at the fold line 71 to form an operable electronic device (see, e.g., fig. 3).**

Applicant respectfully disagrees with the Examiners assertion. Again, the Examiner equates portion **71** of attached Figure 3 to the at least one fold line of the recited invention. Looking at the attached Figure 3 of Nicewarner, Applicant fails to see how portion **71** of Nicewarner defines the alignment of memory arrays on first and second sections wherein the sections may be folded on each other ***at the fold line*** to form an operable electronic device. Stated another way, Nicewarner does not disclose the formation of an operable electronic device by folding first and second layers of memory arrays on each other at portion **71**.

Applicant therefore asserts that since Nicewarner does not disclose the formation of an operable electronic device by folding first and second layers of memory arrays on each other at the fold line as recited in claim 12 of the present invention, claim 12 of the present invention is allowable over the Examiner's cited reference.

Since claims 13-15 are dependent on claim 12, the above-articulated argument with regard to claim 12 applies with equal force to claims 13-15. Accordingly, claims 13-15 should be allowed over this reference.

103 Rejections

The Examiner states:

> **Claims 6, 7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicewarner in view of Schantz (US 5453769).**

Claims 6, 7 and 9

Since claims 6, 7 and 9 are dependent on claim 1, the above-articulated argument with regard to claim 1 applies with equal force to claims 6, 7 and 9. Accordingly, claims 6, 7 and 9 should be allowed over this reference.

Claim 16

The Examiner states:

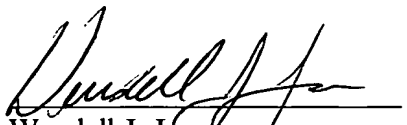
> **Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nicewarner in view of Chauvel (US 4623986).**

Since claim 16 is dependent on claim 12, the above-articulated argument with regard to claim 12 applies with equal force to claim 16. Accordingly, claim 16 should be allowed over this reference.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "Version with markings to show changes made."

Applicant believes that this application is in condition for allowance. Accordingly, Applicant respectfully requests reconsideration, allowance and passage to issue of the claims as now presented. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,



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VERSIONS WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE

AN ASSEMBLY STRUCTURE FOR A MEMORY DEVICE [PORTABLE INEXPENSIVE RUGGED MEMORY, ASSEMBLY STRUCTURES AND METHODS OF FABRICATING SAME]

IN THE CLAIMS

Cancel claim 3.

4. (Twice Amended) The assembly structure recited in claim 1 wherein [at least] one of the [sections] layers of memory arrays [forming each interfaces] comprises conductor line patterns.

5. (Twice Amended) The assembly structure recited in claim 1, wherein the sections forming at least one interface combine to provide a plurality of conductors [and semiconductor patterns].

19. (New) An assembly structure for a memory device, comprising:

a common substrate having multiple sections;

a first layer of a memory array disposed on a first section of the multiple sections wherein the first layer of the memory array comprises a first plurality of conductor lines;

a second layer of a memory array disposed on a second section of the multiple sections wherein the second layer of the memory array comprises a second plurality of conductor lines;

at least one fold line disposed on the common substrate to define alignment of the memory arrays on the first and second sections;

wherein the sections may be folded on each other at the at least one fold line to form an operable electronic device in the memory device;

wherein at least one of the first and second layers of the memory array comprises semiconductor materials and patterns thereon to form a matrix of memory cells; and

wherein the first and second sections are folded along the at least one fold line so that the layers of the memory array are in contact with each other.

20. (New) The assembly structure recited in claim 19 wherein the first plurality of conductor lines are fabricated with first narrowing cross-section areas at points where the memory cells are capable of a permanent change of state.

21. (New) The assembly structure recited in claim 20, wherein the second plurality of conductor lines includes second narrowing cross-section areas configured to align with the first narrowing cross-section areas.